REMARKS

Applicant submits this Amendment, together with a Request for Continued Examination, in response to the Office Action mailed on May 3, 2005, in which claims 1 and 5-8 were rejected. Claims 1, 5 and 7 are amended herewith. Also submitted herewith is a Petition For Extension of Time Under 37 CFR 1.136(a).

In Item 3 of the May 3, 2005 Office Action, claims 1 and 5-8 were rejected under 35 U.S.C. 102(b) as being anticipated by Pilo (US 5,343,428). The Examiner refers to paragraph 4 of the December 1, 2004 Office Action for the details of this rejection. Although Applicant disagrees with the rejection of Claim 1, said claim is amended herewith to clarify what is claimed in order to expedite prosecution of the application. Claim 1 as amended is directed to:

1. A sense amplifier, comprising:
    a sampling circuit receiving an input signal to the sense amplifier;
    a reference node operable to store a reference signal corresponding to the
input data, the reference signal serving as a reference voltage of the sense
amplifier; and
    a timing circuit activating the sampling circuit a predetermined interval
before measurement of the input signal is initiated, the sampling circuit admitting
the input signal to the reference node thereby.

In paragraph 4 of the 12/1/04 Office Action, the Examiner asserts that the "reference node" of claim 1 reads on node 101 or 102 of Pilo. Applicant respectfully disagrees. Nodes 101 and 102 of Pilo are not reference nodes of the differential amplifier 25, operable to store a reference signal. Claim 1 is amended herewith to clarify that "the reference signal serv(es) as a reference voltage of the sense amplifier." The terms "reference node," "reference signal" and reference voltage" are terms of art that are well understood, by those of skill in the art of sensing amplifiers. In the 5/3/05 Office Action, the Examiner argues that nodes 101 and 102 of Pilo are reference nodes "because they are performing the same function/operation as applicant's 'reference' nodes, i.e., if applicant's node 1021 is a reference node, then so too is node 101 (or 102) of Pilo." Applicant respectfully submits that nodes 101 and 102 of Pilo do not, in fact,

perform the same function/operation as the reference node of claim 1 or reference node 1021 in FIG. 10. Specifically, nodes 101 and 102 do not function to store a reference voltage of the differential amplifier 25. Furthermore, Applicant submits that because differential amplifier 25 of Pilo is a *differential* amplifier, it does not make use of a reference voltage at all. Instead, the differential amplifier 25 compares the two input signals to each other, rather than comparing an input signal to a reference signal. Therefore, Applicant respectfully submits that nodes 101 and 102 of Pilo are not reference nodes. Similarly, the "sampling circuit" of Pilo does not admit the input signal (MUXLAT or MUXLAT*) to a reference node. Therefore, Applicant submits that claim 1 is not anticipated by Pilo.

Additionally, the "timing circuit" of Pilo does not activate the "sampling circuit" a predetermined interval before measurement of the input signal is to be taken, as called for in claim 1. Rather, the "timing circuit" merely activates the taking of said measurement when the measurement is to be taken. Referring to FIG. 2 and column7, lines 51-60 of Pilo, the transition of the CLK signal from low to high at time t4 causes the transfer gates 43 and 52 (the "sampling circuit") to become conductive and the input signals MUXLAT and MUXLAT* are allowed to propagate through the BICMOS sense amplifier 20, as indicated by the successive transitions of the voltage levels of node 101, node 102, node 103, node 104 and output signals PED and PED* after time t4. The Examiner asserts that "the input signal MUXLAT* is provided to node 102 prior to the sense amplifier comparison." Applicant disagrees. Rather it is the transition of the CLK signal from low to high that causes the input signals MUXLAT and MUXLAT* to be admitted to the differential amplifier 25, as indicated by the transitions of the voltage levels of node 101, node 102, node 103, node 104 and output signals PED and PED* after time t4. In this scenario, Applicant submits that the measurement of the input signal is "taken" in Pilo when the CLK signal transitions from low to high (see FIG. 2). Of course, the value of the output signals PED and PED* do not change instantaneously upon the CLK transition (though nearly so); the propagation of the signal through nodes 101 and 102, and then through nodes 103 and 104, takes a finite (though very small) amount of time. Therefore, to clarify claim 1, the claim is amended

5

herewith to say that the timing circuit activates the sampling circuit "a predetermined interval before measurement of the input signal is *initiated*." In Pilo, the activation of the "sampling circuit" (transfer gates 43 and 52) and the initiation of the measurement of the input signal are one and the same. Therefore, the timing circuit clearly does not activate the sampling circuit a predetermined interval before measurement of the input signal is initiated, as called for in claim 1. Thus Applicant submits that claim 1 further differentiates over Pilo.
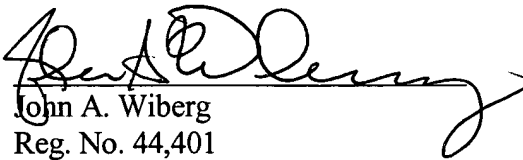
Claim 5 is similar to claim 1 and was rejected under the same grounds as claim 1. Therefore, Applicant submits that claim 5, and claims 6-8 depending therefrom, are not anticipated by Pilo for at least the reasons set forth above with respect to claim 1.

In view of the foregoing, Applicant respectfully requests reconsideration and allowance of claims 1 and 5-8.

The Commissioner is hereby authorized to charge $1,810 (to cover the RCE fee of $790 and the Petition For Extension of Time Fee of $1,020) and any additional fees or credit any overpayment to the deposit account of McAndrews, Held & Malloy, Account No. 13-0017.

Date: <u>November 3, 2005</u>   Respectfully submitted,

John A. Wiberg
Reg. No. 44,401
Attorney for applicants

McANDREWS, HELD & MALLOY, LTD.
500 W. Madison, Suite 3400
Chicago, IL 60661
Telephone: 312 775 8000